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Bibliography.

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* NOTICES *



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Summary.

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(57) [Abstract]
[Technical problem] When it is made to connect by the borderless contact hole, it incorrect-connects too hastily, or it aims at making it a poor proof pressure not occur.
[Means for Solution] In the semiconductor device which was made to perform multilevel-metal wiring 3, 8, and 14, the difficulty etching layer 20 which consists of SiN, SiON, SiC, SiCN, etc. which contain N or C in the interstitial segment of the lower layer insulating layer of the metal wiring 8 is formed on the semiconductor substrate 1.

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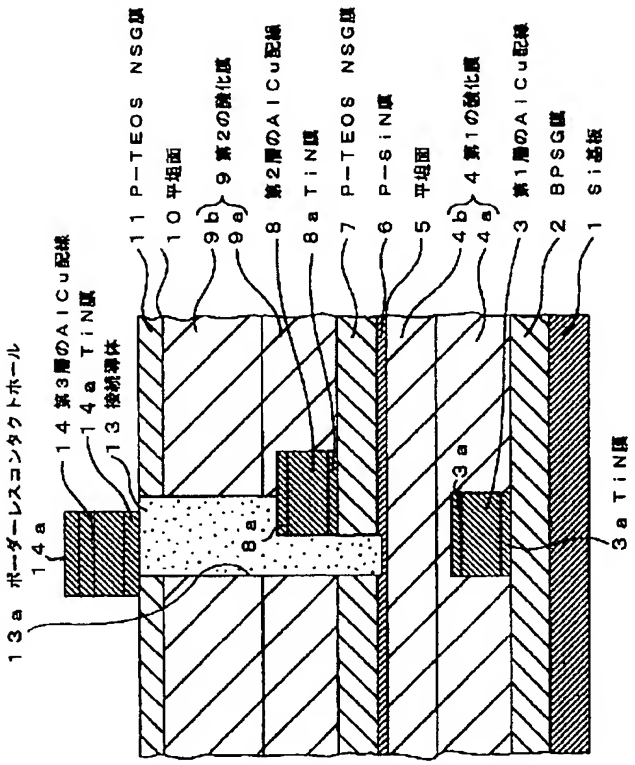


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[Translation done.]

* NOTICES *

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3.In the drawings, any words are not translated.

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CLAIMS

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[Claim(s)]

[Claim 1] The semiconductor device characterized by preparing the difficulty etching layer which consists of SiN, SiON, SiC, SiCN, etc. which contain N or C in the interstitial segment of the lower layer insulating layer of metal wiring in the semiconductor device which was made to perform multilevel-metal wiring on a semiconductor substrate.

[Claim 2] The semiconductor device characterized by considering as the etching stop layer in the case of etching of the difficulty etching layer which consists of SiN, SiON, SiC, SiCN, etc. containing Above N and C in a semiconductor device

according to claim 1 of the contact hole of a high aspect ratio.
[Claim 3] It is the difficulty etching layer which consists of SiN, SiON, SiC, SiCN, etc. containing Above N and C in a semiconductor device according to claim 1 C+ Or N+ Semiconductor device characterized by forming by carrying out an ion implantation.

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* NOTICES *



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## DETAILED DESCRIPTION

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[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] this invention is applied to for example, VLSI equipment, and relates to a suitable semiconductor device.
[0002]
[Description of the Prior Art] In order to attain each constituent child's reduction in accordance with high integration of a semiconductor device in recent years, the continuation **** borderless contacting method which used the contact hole which does not have the degree of margin in the interconnection between each of this constituent child is being used.
[0003] the time of processing a contact hole by this borderless contacting method -- C4 F8 / CO/Ar, CHF3 / CO/Ar, and C4 F8 / CO/Ar/O2 etc. -- magnetron reactive ion etching (magnetron RIE) using mixed gas is used
[0004] In this magnetron RIE, since processing conditions are set up so that the selection ratio of a high opposite resist, opposite TiN, and TiW and W and good mu-loading effect may be obtained, a borderless contact hole with a high aspect ratio with the good (theta= 88 degrees - 90 degrees) angle control with few size conversion differences can be obtained.
[0005]
[Problem(s) to be Solved by the Invention] Since mu-loading effect to the contact hole of a detailed path (phi= 0.50 micrometers or less) is raised in this magnetron RIE, More than advance (omission nature) of etching of the oxide film which constitutes the insulator layer of the portion which forms a borderless contact hole expected, are good. For example, as shown in drawing 7 , when it is going to obtain the contact hole to the metal wiring (AlCu wiring) 8, the phenomenon in which the pars basilaris ossis occipitalis of this contact hole 13a reaches to the

lower layer of this AlCu wiring 8 is seen (a metal wiring lower layer should dig).
[0006] The short circuit and poor proof pressure between multilayer interconnections etc. occurred by this, and there was un-arranging [ which cannot acquire a good electrical property ].
[0007] Furthermore, with reference to drawing 7 , it attaches inconvenient [ this former ] and explains. Si substrate by which, as for 1, accumulation formation of the transistor etc. was carried out in drawing 7 , the boron phosphorus SHIRIKEDO glass (BPSG) film by the reflow from which 2 constitutes an insulator layer, The titanium night RAIDO (TiN) film with which 3 put the 1st-layer AlCu wiring and 3a on the upper and lower sides of this 1st-layer AlCu wiring 3, 4 is P-TEOS formed by the plasma CVD which constitutes a layer insulation film. A NSG film and O3-TEOS The 1st oxide film which consists of two-layer [ with a NSG film ], 7 is P-TEOS. The insulator layer which consists of a NSG film, and 8 The 2nd-layer AlCu wiring, 9 is the TiN film which put 8a on the upper and lower sides of this 2nd-layer AlCu wiring, and P-TEOS which constitutes a layer insulation film. A NSG film and O3-TEOS The 2nd oxide film which consists of two-layer [ with a NSG film ], 11 is P-TEOS. The insulator layer which consists of a NSG film, and 14 are the TiN films which put the 3rd-layer AlCu wiring and 14a on the upper and lower sides of this 3rd-layer AlCu wiring 14.
[0008] In the example of **** drawing 7 to connect the 2nd-layer AlCu wiring 8 and the 3rd-layer AlCu wiring 14 When borderless contact hole 13a is formed by this magnetron RIE As it is good more than advance (omission nature) of this etching expected, and the bottom of this contact hole 13a shows drawing 7 the connection formed by CVD and the etchback method when it had reached to the 1st-layer AlCu wiring 3 -- a conductor (for example, W plug) 13 produces un-arranging [ which also incorrect-short-circuits the 1st-layer AlCu wiring 3 ]
[0009] It incorrect-connects too hastily or this invention aims at making it a poor proof pressure not occur, when it is made to connect by the borderless contact hole in view of ******.
[0010]
[Means for Solving the Problem] this invention semiconductor device prepares the difficulty etching layer which consists of SiN, SiON, SiC, SiCN, etc. which contain N or C in the interstitial segment of the lower layer insulating layer of metal wiring in the semiconductor device which was made to perform multilevel-metal wiring on a semiconductor substrate.
[0011] Since the difficulty etching layer which consists of SiN, SiON, SiC, SiCN, etc. containing N or C by **** and this invention turns into an etching stop layer at the time of forming the contact hole of the high aspect ratio in Magnetron RIE, when it is made to connect by this borderless contact hole, it is between multilevel-metal wiring, and an incorrect short circuit is not produced or a poor proof pressure does not occur.
[0012]
[Embodiments of the Invention] With reference to drawing 1 - drawing 3 , an example of the form of operation of this invention semiconductor device is explained according to the example of manufacture below. In this drawing 1 - drawing 3 , the same sign is attached and shown in the portion corresponding to

drawing 7 .
[0013] In this example, as first shown in drawing 2 , a transistor etc. forms the boron phosphorus SHIRIKEDO glass (BPSG) film 2 by the reflow which constitutes an insulator layer on the Si substrate 1 by which accumulation formation was carried out. On this BPSG film 2, micro processing of the 1st-layer AlCu wiring 3 which made this BPSG film 2 the ground is carried out by dry etching, and it is formed. In this case, it carries out as [ put / TiN film 3a / on the vertical side of this 1st-layer AlCu wiring 3 ]. Thickness of this 1st-layer AlCu wiring 3 is set to about 500nm.
[0014] P-TEOS formed by the plasma CVD method on this AlCu wiring 3 and BPSG film 2 of the 1st layer NSG film 4a and O3-TEOS The 1st oxide film 4 which constitutes the layer insulation film which consists of two-layer [ of NSG film 4b ] is formed.
[0015] Then, this 1st oxide-film 4 top is ground by the CMP method, it supposes that it is flat, and the flat side 5 is formed. In this case, thickness of this 1st oxide film 4 is set to about 900nm.
[0016] In this example, it forms as a difficulty etching layer by the plasma CVD method on this flat side 5, the SiN film 6, i.e., the P-SiN film, which are 200nm or less in thickness, and a 100nm insulator layer. As conditions which form this P-SiN film 6, it considered as NH3 / SiH4 / N2 =300/100/3000sccm, 4.0Torr, 600W, and 400 degrees C, and parallel monotonous type plasma CVD equipment was used.
[0017] Next, they are 200nm or less in thickness, and 100nm P-TEOS by the plasma CVD method on this P-SiN film 6. The NSG film 7 is formed. This P-TEOS As conditions which form the NSG film 7, it considered as O2 / TEOS=500/900sccm, 8.0Torr, 800W, and 400 degrees C, and parallel monotonous type plasma CVD equipment was used.
[0018] This P-TEOS It is this P-TEOS on the NSG film 7. Micro processing of the 2nd-layer AlCu wiring 8 which made the NSG film 7 the ground is carried out by dry etching, and it is formed. In this case, it carries out as [ put / TiN film 8a / on the vertical side of this 2nd-layer AlCu wiring 8 ]. Thickness of this 2nd-layer AlCu wiring 8 is set to about 500nm.
[0019] This 2nd-layer AlCu wiring 8 and P-TEOS P-TEOS formed by the plasma CVD method on the NSG film 7 NSG film 9a and O3-TEOS The 2nd oxide film 9 which constitutes the layer insulation film which consists of two-layer [ of NSG film 9b ] is formed.
[0020] Then, this 2nd oxide-film 9 top is ground by the CMP method, it supposes that it is flat, and the flat side 10 is formed. In this case, thickness of this 2nd oxide film 9 is set to about 900nm.
[0021] They are 200nm or less in thickness, and 100nm P-TEOS by the plasma CVD method on this flat side 10. The NSG film 11 is formed.
[0022] This P-TEOS It carries out as [ form / the resist 12 of the magnetron RIE by which the pattern of the borderless contact hole of a predetermined number was formed on the NSG film 11 ].
[0023] Next, this resist 12 is used and the borderless contact hole by Magnetron RIE is etched. Here, 1.5-micrometer etching of a high aspect ratio is carried out

by depth conversion including a part for the over etching of the thickness of the deepest layer insulation film. It is carrying out as [ acquire / a good property / by optimizing etching conditions / to mu-loading effect, the selection ratio for a resist, the selection ratio for TiN, angle control, etc. ].
[0024] The conditions of this etching are C4 F8/CO/Ar/O2 =12/100/200/5sccm, 6.0Pa, 1600W, 20 degrees C, and P-TEOS. The selection ratio 25 for NSG=450 nm/min**4.8% and TiN, mu-loading effect = it considers as theta= 88 degrees or more of angle control 85% or more.
[0025] In this case, in contact hole 13a of the shallowest layer insulation thickness, if the bottom of contact hole 13a reaches a depth of 1.1 micrometers (under the 2nd-layer AlCu wiring 8 100nm), as shown in drawing 3 , the P-SiN film 6 will be exposed to the bottom of this contact hole 13a, and advance of this etching will be prevented. This is Cfour F8-/CO/Ar/O2 like common knowledge. SiO2 to SiN It is for the mechanism of high selection-ratio etching to work (refer to JP,6-132252,A).
[0026] Moreover, P-TEOS which is the oxide film of the ground of the 2nd-layer AlCu wiring 8 in shallow contact hole 13a of layer insulation thickness in order that an etching stop with the P-SiN film 6 may work **** of NSG7 gathers in the fixed depth (this example under the 2nd-layer AlCu wiring 8 100nm). In deep contact hole 13a, in order for the amount of over etching to join the thickness of a layer insulation film, contact hole 13a which is a high aspect ratio punctures.
[0027] Then, a resist 12 is removed as shown in drawing 3 by the known method. next, this contact hole 13a -- CVD and the etchback method -- or CVD and the CMP method -- connection -- a conductor (for example, W plug) 13 is formed
[0028] it is shown in drawing 1 -- as -- connection of this contact hole 13a -- it connects with the upper surface of a conductor 13 electrically, and micro processing of the 3rd-layer AlCu wiring 14 is carried out by dry etching, and it is formed In this case, it carries out as [ put / TiN film 14a / on the vertical side of this 3rd-layer AlCu wiring 14 ]. Thickness of this AlCu wiring 14 is set to about 500nm.
[0029] Since the P-SiN film 6 is used as the etching stop film while being able to form borderless contact hole 13a of a high aspect ratio good, since mu-loading effect is improved according to this example, when the 3rd-layer AlCu wiring 14 and the 2nd-layer AlCu wiring 8 are connected using this borderless contact hole 13a, an incorrect short circuit is not produced, or a poor proof pressure does not occur.
[0030] That is, according to this example, since between the 1st-layer AlCu wiring 3 and the bottoms of borderless contact hole 13a is set as 400nm or more, about [ that an incorrect short circuit does not arise ] and pressure-proofing between layers is also secured, and there are profits which can acquire a good electrical property.
[0031] Therefore, when this example is applied to VLSI equipment, there are profits which can obtain VLSI equipment with good reliability for high quality.
[0032] In addition, although the above-mentioned example was attached and stated to the example which used the SiN film 6 (P-SiN film by plasma CVD) as a difficulty etching layer, of course, the thin film containing N, such as SiON and

SiOFN, can instead be used.
[0033] Moreover, although plasma CVD equipment was used for forming membranes in the above-mentioned example, of course, high-density CVD systems, such as an efficient consumer response (Electoron Cyclotron Resonance) CVD system, a helicon wave CVD system, and an ICP (Inductively Coupled Plasma) CVD system, can instead be used.
[0034] Next, with reference to drawing 4 , drawing 5 , and drawing 6 , it explains per other examples of the gestalt of operation of this invention. In this drawing 4 , drawing 5 , and drawing 6 , the same sign is attached and shown in the portion corresponding to drawing 1 , drawing 2 , and drawing 3 .
[0035] In this example, as first shown in drawing 4 , a transistor etc. forms the boron phosphorus SHIRIKEDO glass (BPSG) film 2 by the reflow which constitutes an insulator layer on the Si substrate 1 by which accumulation formation was carried out. On this BPSG film 2, micro processing of the 1st-layer AlCu wiring 3 which made this BPSG film 2 the ground is carried out by dry etching, and it is formed. In this case, it carries out as [ put / TiN film 3a / on the vertical side of this 1st-layer AlCu wiring 3 ]. Thickness of this 1st-layer AlCu wiring 3 is set to about 500nm.
[0036] P-TEOS formed by the plasma CVD method on this AlCu wiring 3 and BPSG film 2 of the 1st layer NSG film 4a and O3-TEOS The 1st oxide film 4 which constitutes the layer insulation film which consists of two-layer [ of NSG film 4b ] is formed.
[0037] Then, this 1st oxide-film 4 top is ground by the CMP method, it supposes that it is flat, and the flat side 5 is formed. In this case, thickness of this 1st oxide film 4 is set to 500nm - 900nm.
[0038] Then, it sets to this example and is N+ from this flat side 5. An ion implantation is carried out all over a wafer, and the difficulty etching layer 20 which consists of SiN is formed. This N+ that carried out the ion implantation Average projection range Rp 100nm or less is suitable from this flat side 5. This average projection range Rp Standard deviation deltaRp Since it is about **30nm, the layer mixed by high concentration is formed in about 60nm (although the mixing layer after pouring is amorphous, it polycrystal-izes by heating under membrane formation of ******, and SiN, SiON mixed crystal, etc. generate.).
[0039] This N+ Ion-implantation conditions are acceleration energy 100KeV, N+=1E16cm2, and room temperature pouring.
[0040] Next, it is 100nm P-TEOS by the plasma CVD method on this flat side 5. The NSG film 7 is formed. This P-TEOS As conditions which form the NSG film 7, it considered as O2-/TEOS=500/900sccm, 8.0Torr, 800W, and 400 degrees C, and parallel monotonous type plasma CVD equipment was used.
[0041] This P-TEOS It is this P-TEOS on the NSG film 7. Micro processing of the 2nd-layer AlCu wiring 8 which made the NSG film 7 the ground is carried out by dry etching, and it is formed. In this case, it carries out as [ put / TiN film 8a / on the vertical side of this 2nd-layer AlCu wiring 8 ]. Thickness of this 2nd-layer AlCu wiring 8 is set to about 500nm.
[0042] This 2nd-layer AlCu wiring 8 and P-TEOS P-TEOS formed by the plasma CVD method on the NSG film 7 NSG film 9a and O3-TEOS The 2nd oxide film 9

which constitutes the layer insulation film which consists of two-layer [ of NSG film 9b ] is formed.
[0043] Then, this 2nd oxide-film 9 top is ground by the CMP method, it supposes that it is flat, and the flat side 10 is formed. In this case, thickness of this 2nd oxide film 9 is set to 500nm - 900nm. They are 200nm or less in thickness, and 100nm P-TEOS by the plasma CVD method on this flat side 10. The NSG film 11 is formed.
[0044] This P-TEOS It carries out as [ form / the resist 12 of the magnetron RIE in which the pattern which forms the borderless contact hole of a predetermined number on the NSG film 11 was formed ].
[0045] Next, this resist 12 is used and the borderless contact hole by Magnetron RIE is etched. Here, 1.5-micrometer etching of a high aspect is carried out by depth conversion including a part for the over etching of the thickness of the deepest layer insulation film. It is carrying out as [ acquire / a good property / by optimizing this etching condition / to mu-loading effect, the selection ratio for a resist, the selection ratio for TiN, angle control, etc. ].
[0046] This etching condition is C4 F8/CO/Ar/O2 =12/100/200/5sccm, 6.0Pa, 1600W, 20 degrees C, and P-TEOS. The selection ratio 25 for NSG=450 nm/min**4.8% and TiN, mu-loading effect = it considers as theta= 88 degrees or more of angle control 85% or more.
[0047] In this case, in contact hole 13a of the shallowest layer insulation film, if the bottom of this contact hole 13a reaches a depth of 1.1 micrometers (under the 2nd-layer AlCu wiring 8 100nm), as shown in drawing 5 , the difficulty etching layer 20 of SiN and SiON will be exposed to a bottom, and advance of this etching will be prevented. This is C4 F8 / Co/Ar/O2 like common knowledge. SiO2 to SiN It is for the mechanism of high selection-ratio etching to work (refer to JP,6-132252,A).
[0048] Moreover, in order that an etching stop in the difficulty etching layer 20 of SiN and SiON may work in shallow contact hole 13a of the thickness between layers, it is the depth (it gathers in about 200nm under AlCu wiring) with fixed **** of the oxide film of the ground of wiring. in order for the amount of over etching to join the thickness of a layer insulation film in deep contact hole 13a -- high -- an aspect contact hole punctures
[0049] Then, a resist 12 is removed as shown in drawing 5 by the known method. next, this contact hole 13a -- CVD and the etchback method -- or CVD and the CMP method -- connection -- a conductor (for example, W plug) 13 is formed
[0050] it is shown in drawing 6 -- as -- connection of this contact hole 13a -- it connects with the upper surface of a conductor 13 electrically, and micro processing of the 3rd-layer AlCu wiring 14 is carried out by dry etching, and it is formed In this case, it carries out as [ put / TiN film 14a / on the vertical side of this 3rd-layer AlCu wiring 14 ]. Thickness of this AlCu wiring 14 is set to about 500nm.
[0051] Since the difficulty etching layer 20 of SiN and SiON is used as the etching stop layer while being able to form borderless contact hole 13a of a high aspect ratio good, since mu-loading effect is improved according to this example When **** of a contact hole is stopped by this and the 3rd-layer AlCu wiring 14

and the 2nd-layer AlCu wiring 8 are connected using this borderless contact hole 13a, an incorrect short circuit is not produced, or a poor proof pressure does not occur.
[0052] Moreover, according to this example, it is N+. The difficulty etching layer 20 of arbitrary SiN(s) and SiON can be formed by setting the pouring conditions of ion as a desired value.
[0053] in addition, the above-mentioned example -- setting -- N+ although attached and stated to the example which poured in ion and formed the difficulty etching layer of SiN and SiON -- instead of [ this ] -- C+ ion is poured in and good also as a difficulty etching layer of SiC -- carrying out -- moreover, C+ Ion and N+ Even if it forms the difficulty etching layer of SiCN by double injection of ion, he can understand easily what the same operation effect as **** is acquired for.
[0054] This C+ The examples of the conditions of an ion implantation are 100KeV(s), C+=1E16cm2, and room temperature pouring.
[0055] Moreover, this invention of the ability of various composition to take is natural, without deviating from the summary of this invention, without restricting to the above-mentioned example.
[0056]
[Effect of the Invention] Since according to this invention mu-loading effect is improved, and the difficulty etching layer which consists of SiN, SiON, SiC, SiCN, etc. containing N or C is used as the etching stop layer while being able to form the borderless contact hole of a high aspect ratio good, the position of the bottom of this borderless contact hole is decided, and there are profits which do not produce an incorrect short circuit when connecting between multilevel-metal wiring by this borderless contact hole, or a poor proof pressure does not generate.
[0057] Therefore, according to this example, it is quality and there are profits which can obtain semiconductor devices, such as a VLSI element with good reliability.

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[Translation done.]

* NOTICES *


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2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

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DESCRIPTION OF DRAWINGS

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[Brief Description of the Drawings]
[Drawing 1] It is the cross section showing an example of this invention

semiconductor device.
[Drawing 2] It is the cross section showing the example of a manufacturing process of drawing 1 .
[Drawing 3] It is the cross section showing the example of a manufacturing process of drawing 1 .
[Drawing 4] It is the cross section showing the example of a manufacturing process of other examples of this invention.
[Drawing 5] It is the cross section showing the example of a manufacturing process of other examples of this invention.
[Drawing 6] It is the cross section showing other examples of this invention.
[Drawing 7] It is the cross section with which explanation of the example of the conventional semiconductor device is presented.
[Description of Notations]
a 1 --Si substrate, a 2 --BPSG film, and 3 -- -- the 1st-layer AlCu wiring, the 4 -- 1st oxide film, 5, and 10 -- -- a flat side, a 6 --P-SiN film, 7, and 11 --P-TEOS a NSG film and 8 -- -- the 2nd-layer AlCu wiring and 9 -- -- the 2nd oxide film, 12 -- resist, and 13 -- connection -- a conductor, a 13a-- borderless contact hole, and 14 -- -- layer AlCu

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DRAWINGS

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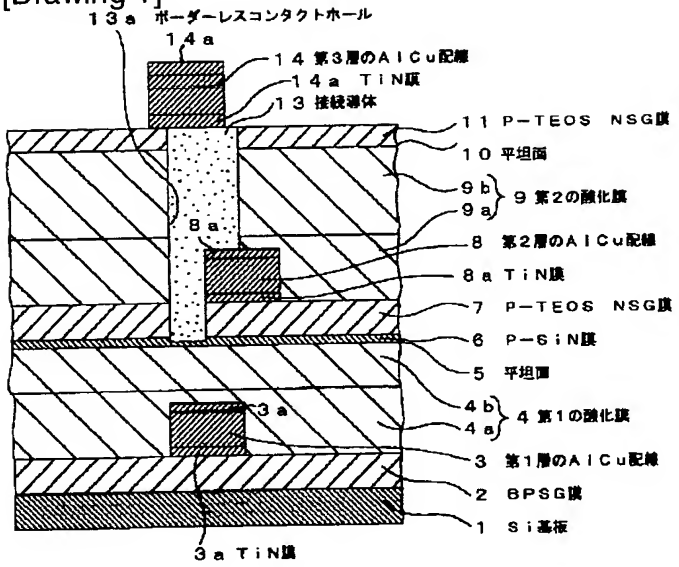
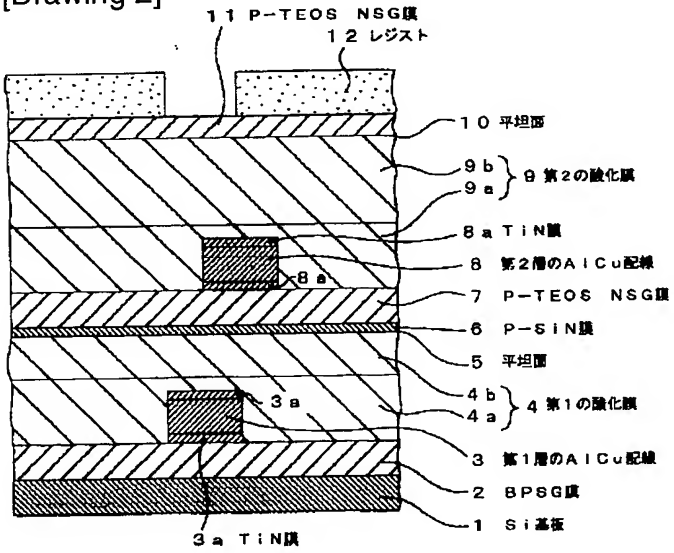
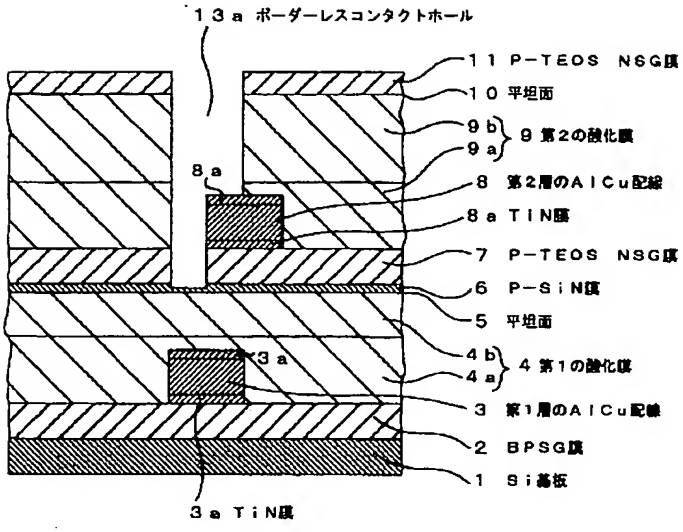
[Drawing 1]



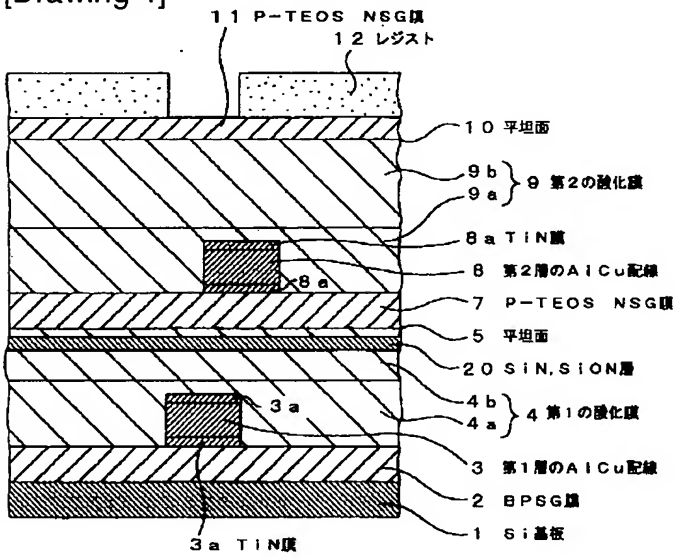

[Drawing 2]



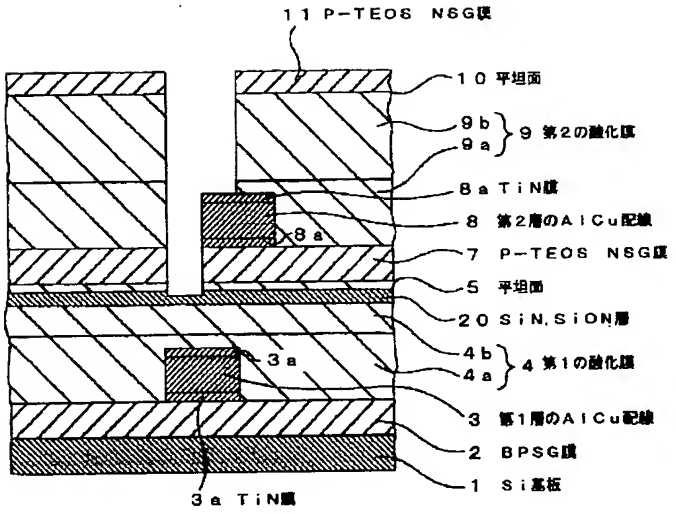

[Drawing 3]



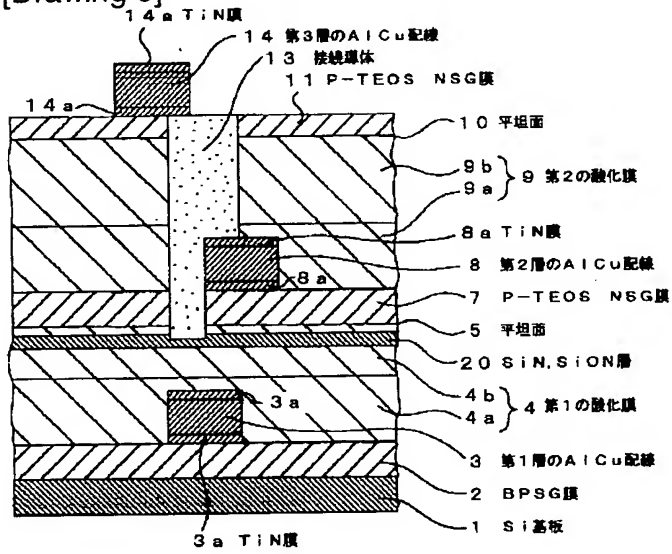

[Drawing 4]



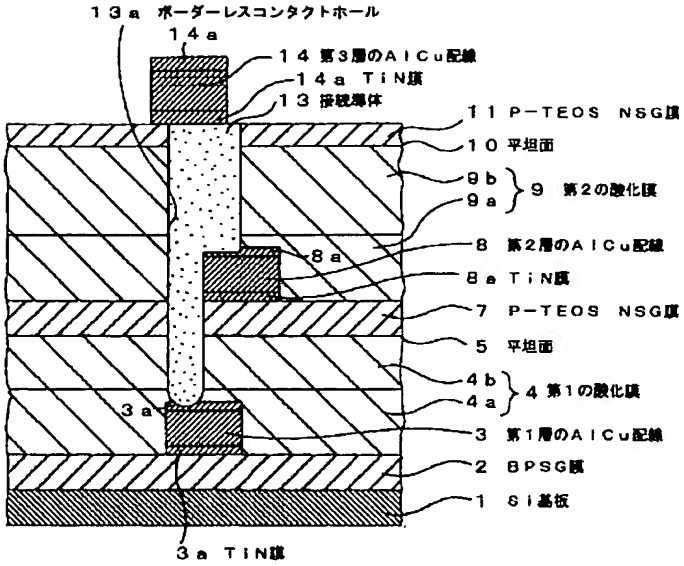

[Drawing 5]




[Drawing 6]




[Drawing 7]

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